What is Claimed is:

1. A quarter-rate phase detector comprising:

four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals;

an error circuit to combine corresponding ones of the latched signals, respectively, resulting in a plurality of intermediate signals; and

a multiplexing unit to selectively output the intermediate signals as a phase error signal.

2. The quarter-rate phase detector of claim 1, wherein:

the quadrature clock signals include signals I, Q, Ib and Qb;

a first one of the latches is controlled by I;

a second one of the latches is controlled by Q;

a third one of the latches controlled by Ib; and

a fourth one of the latches is controlled by Qb.

3. The quarter-rate phase detector of claim 1, wherein the multiplexing unit is controllable by the quadrature clock signals.

4. The quarter-rate phase detector of claim 1, wherein the multiplexing unit is controllable to truncate the intermediate signals.

5. The quarter-rate phase detector of claim 4, wherein the multiplexing unit is operable to form the phase error signal by cycling through the truncated intermediate signals.

6. The quarter-rate phase detector of claim 1, wherein:

the quadrature clock signals include signals I and Q; and

the multiplexing unit is controlled according to the signals I and Q, respectively.

7. The quarter-rate phase detector of claim 6, wherein the multiplexing unit includes:

a first multiplexer and a second multiplexer to receive the intermediate signals, respectively; and

a third multiplexer to multiplex outputs of the first and second multiplexers.

8. The quarter-rate phase detector of claim 1, wherein

the corresponding latched signals are pairs of latched signals; and

each pair has a first set and a second set, the second set representing the latched signals subsequently closest in time to the first set, respectively.

9. The quarter-rate phase detector of claim 8, wherein:

the error circuit includes four exclusive OR (XOR) gates, each XOR gate receiving one of the pairs, respectively.

10. The quarter-rate phase detector of claim 1, wherein:

the four latches represent a first set of latches and the latched signals represent a first set of latched signals;

the detector further comprises:

a second set of four latches arranged to receive the outputs of the first set of latches, respectively, and controllable to latch data at different times according to the quadrature clock signals, respectively, so as to form a second set of latched signals; and

the second set representing re-timed versions of the received data.

11. The quarter-rate phase detector of claim 10, wherein:

the second set of latched signals is organized as pairs;

the detector further comprises:

a reference circuit to generate a reference signal based upon transitions in the second set of latched signals.

12. The quarter-rate phase detector of claim 11, wherein:

the second set of latched signals is organized as pairs;

the reference circuit includes:

a plurality of multiplexers to selectively output the pairs of re-timed data; and

an exclusive OR (XOR) gate to receive the outputs of the plurality of multiplexers.

13. The quarter-rate phase detector of claim 1, wherein the rate of the intermediate signals is ¼ of the received data rate.

14. A quarter-rate phase detector comprising:

four data latches, each latch receiving the same input data, the latches being clocked by quadrature clock signals, respectively, so as to produce latched signals; and

an error signal-generating circuit to generate a phase error signal based upon the four latched signals and the quadrature clocks signals.

15. The quarter-rate phase detector of claim 14, wherein the error-signal-generating circuit is operable upon the four latched signals and is controlled by the quadrature clocks signals.

16. A quarter-rate phase detector comprising:

four XOR gates receiving latched signals, each latched signal corresponding to input data latched according to one of quadrature clock signals, respectively, each XOR gate generating an intermediate signal;

a multiplexer to selectively output one of the four intermediate signals as a phase error signal.

17. The quarter-rate phase detector of claim 16, further comprising:

four data latches, each latch receiving the same input data, the latches being clocked by quadrature clock signals, respectively, so as to produce quadrature latched data signals;

18. A clock and data recovery (CDR) circuit comprising:

a phase-error generating circuit to determine quarter-rate phase detector;

a charge pump operable upon an output of the phase detector;

a filter operable upon an output of the charge pump; and

a quadrature voltage-controlled oscillator (VCO) operable upon an output of the filter;

the phase-detector being controllable by the output of the VCO.

19. The CDR circuit of claim 18, wherein the rate of the quadrature signals of VCO is ¼ of the received data rate of the phase-error generating circuit.

20. The CDR circuit of claim 18, wherein the phase-error-generating circuit includes:

four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals;

an error circuit to combine corresponding ones of the latched signals, respectively, the error circuit providing a plurality of intermediate signals; and

a multiplexing unit to selectively output the intermediate signals as a phase error signal.

21. A method of detecting phase at a quarter of the rate of the received data, the method comprising:

latching, at different times according to quadrature clock signals, respectively, the received data so as to form latched signals;

combining corresponding ones of the latched signals, respectively, to provide a plurality of intermediate signals; and

selectively outputting one among the intermediate signals, respectively, to provide a constructed a phase error signal.

22. The method of claim 21, wherein:

the quadrature clock signals include signals I and Q; and

the selectively outputting step selectively outputs according to the signals I and Q, respectively.

23. The CDR circuit of claim 21, wherein the rate of the quadrature clock signals is ¼ of the received data rate.

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